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Design of Optical Imaging Sensor

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Abstract: Optical imaging sensor detects optical signal and converts optical signal into an electrical signal to form an image. This paper discusses design of time delay integration (TDI) Charge Coupled Device (CCD) optical imaging sensor, which is under design, using double – poly double – metal front illuminated (FI) CCD process. TDI is a technique to enhance SNR for a scene, which generate small signal. The pixel architecture will be based on Metal Oxide Semi-Conductor (MOS) capacitor. Detector shall be responsive over 450nm - 900nm wavelength. Detector architecture is primarily driven by EO (electro-optics) parameters and available process. This paper also discusses design parameters, chip architecture, pixel architecture, TDI stage selection option, design of horizontal shift register (HSR).

Keywords: CCD (Charge Coupled Device), High resolution, Imaging sensor, Signal-to-noise ratio, Super resolution, Time delay Integration.

1. INTRODUCTION

TDI imaging sensors are used in applications where a line scan system is required for high quality, low noise and high contrast imaging even under low illumination conditions. In this technique, sensed charge patterns are shifted across the charge-coupled device (CCD) array in synchronization to the movement of the object, to integrate more light from the scene[1]. This technique permits high resolution imaging of fast moving faint objects using low aperture (large F number) optics. Specifications of TDI imaging sensor, which is under design are given in **Table 1.**

Table 1. Sensor specifications

Parameter	Details
Detector type	TDI CCD
Photosensitive elements	7200×160 Pixels
Pixel Pitch	13µm
Pixel Size	Photosensitive size 13 µm X 13 µm, MOS
TDI stage selection	1, 8, 16, 32, 48, 64, 96, 128, 160
Number of TDI arrays in single chip	Two arrays staggered by half pixel
Line Rate	20 kHz
Full well capacity (ke-)	>170
Read noise	≤100
Dark signal non uniformity	≤1%
Photo response non uniformity	≤5%
Vertical Charge transfer Inefficiency	≤2%
Horizontal Charge transfer Inefficiency	≤1%

2. CHIP ARCHITECTURE

Architecture options are primarily driven by device specifications, EO parameters, design rules with respect to metal strapping, and reticle stitching.

This sensor requires two independent TDI CCD array staggered by half pixel in across track direction. Basic architecture for any TDI CCD is very much similar to full frame CCD image sensor.

Basic chip architecture is shown in figure 1. As per requirement array format would be 7200 x160 photosensitive pixels with pixel size 13um x13um and pixel pitch of 13um. As, it is a TDI CCD image sensor with 9 different stage selection options, overflow drain in kept at top of the array near to 160 TDI row.

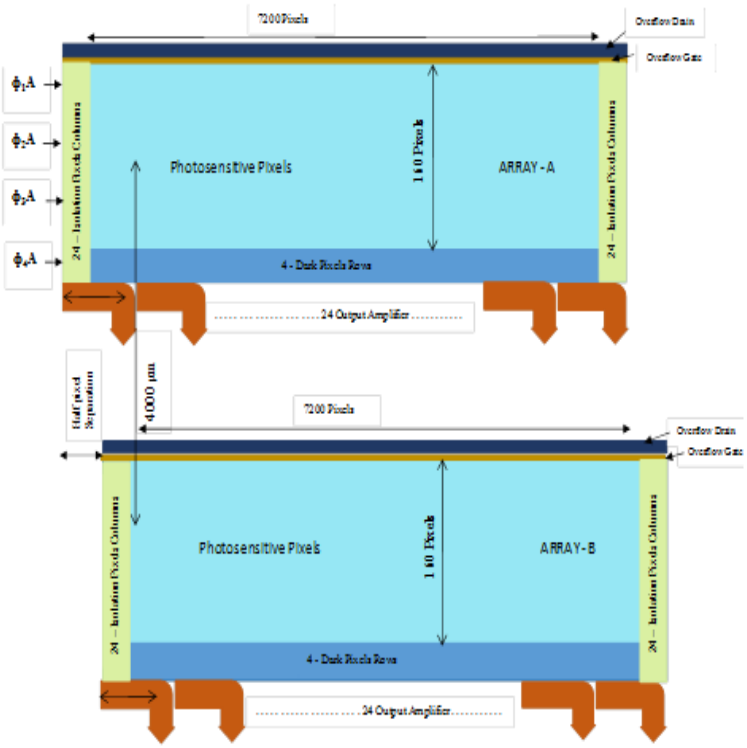


Figure 1. Chip Architecture

Overflow drain potential and TDI blocking gate potential shall be such that charges generated more than well capacity

in unselected TDI stages shall flow towards overflow drain. On both side of image region there are 24 shield columns and 4 shielded rows. Out of 24 shield columns 18 columns are readout as dark reference and 6 columns are dump columns. Vertical shift register design is primarily driven by pixel size, full well capacity and vertical charge transfer efficiency.

Considering full well capacity, vertical CTI and low noise requirement at pixel level four phase pixel architecture is considered. Estimated FWC for 13um x 13um pixel with four phase clocking is >270ke.

To maintain the clock fidelity clocks shall be fed from both sides (left and right) of the image region and pixels are metal strapped in pixel isolation region.

There are 8 TDI stage select lines for selecting 1, 8, 16, 32, 48, 64, 96, 128 & 160 stages respectively. Stage selection is used to select from where the charge transfer and integration would take place when the TDI stage is selected.

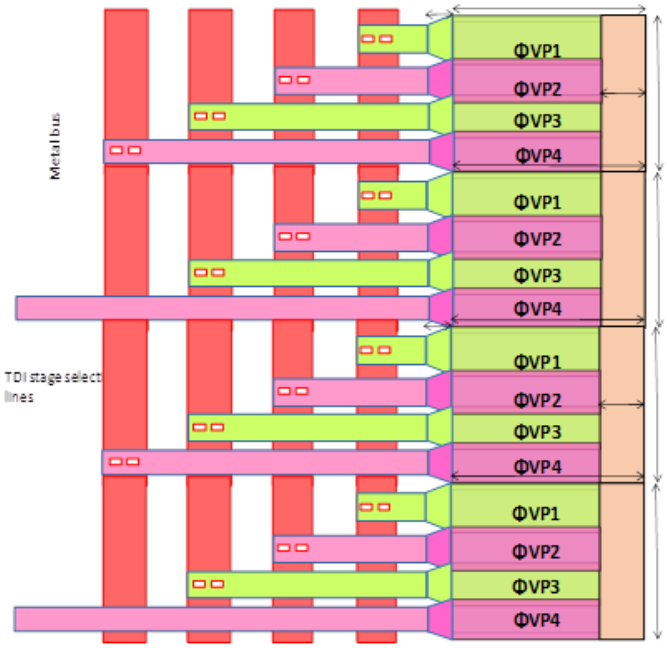


Figure 2. Time Delay Integration (TDI) stages

A. Vertical Shift Register Potential Diagram:

Here, when the TDI Stage is selected, the TDI rows are kept at low voltage at the same time the Dump Gate and Dump Drain are kept at high voltage.

Hence during the charge transfer that is taking place whenever the TDI stage is selected the extra charge is dumped into the Dump drain. It is a four phase potential diagram for vertical shift register.

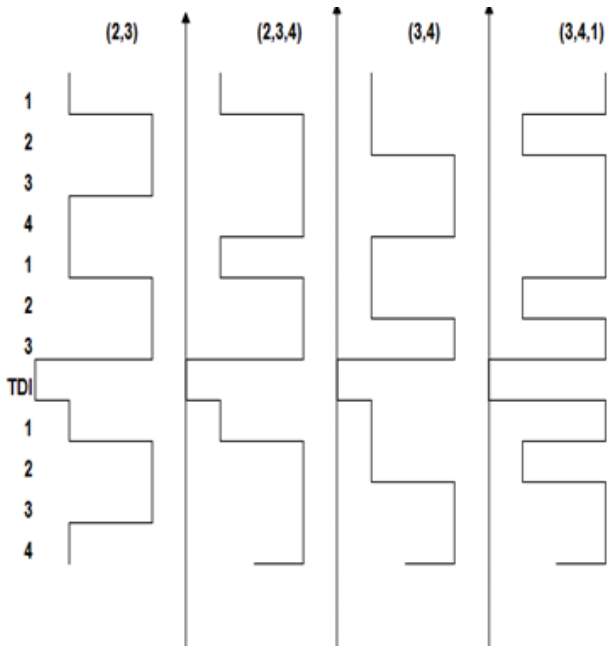


Figure 3. Potential Diagram

The charge from Image Pixel is transferred to Horizontal shift registers (HSR) through transfer clock[2].

HSR is designed to handle twice the pixel capacity.

Considering amplifier operating rate, charges integrated over selected TDI stages are readout through 24 horizontal shift registers. Each shift register read charges of 603 pixels. Two types of HSR design options are considered.

1. Four phase:

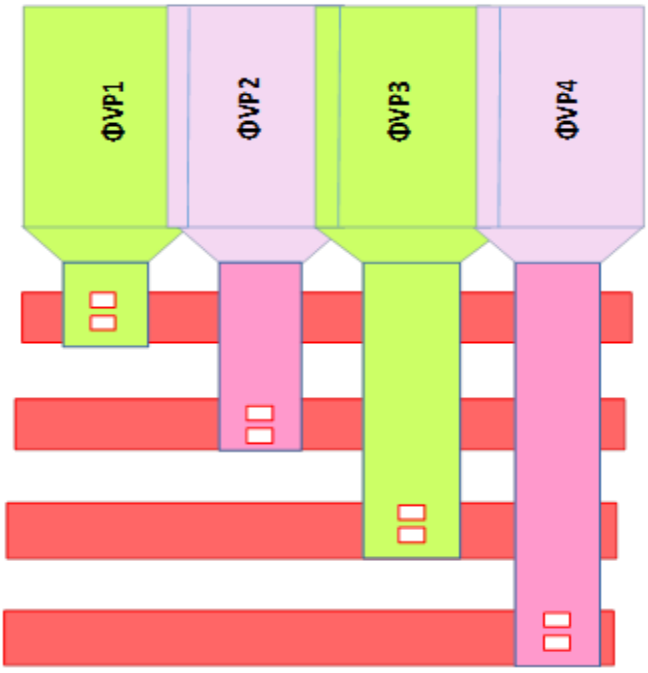


Figure 4. Four Phase HCCD

In four phases HSR, charges are transferred and collected under two phase. It provides better charge handling capacity[1] than two phase HSR, but HSR bus routing becomes complex due to four different phases and 24 HSR buses. In this, bus for

two HSR can be combined maintains separation between two arrays.

2. Two phase:

In two phase architecture charges are stored under single gate and thus width of HSR is more than four phase to accommodate same charge but its routing is less complex.

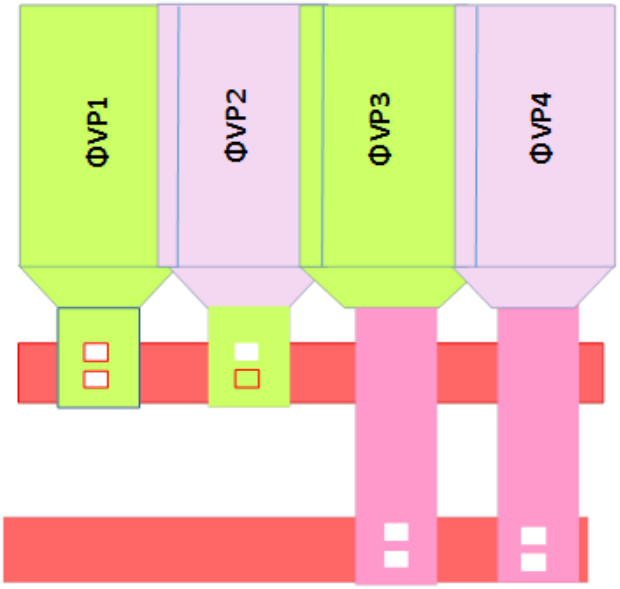


Figure 5. Two Phase HCCD

Considering better CTE and charge handling capacity 4-phase N-buried channel type HSR architecture is chosen.

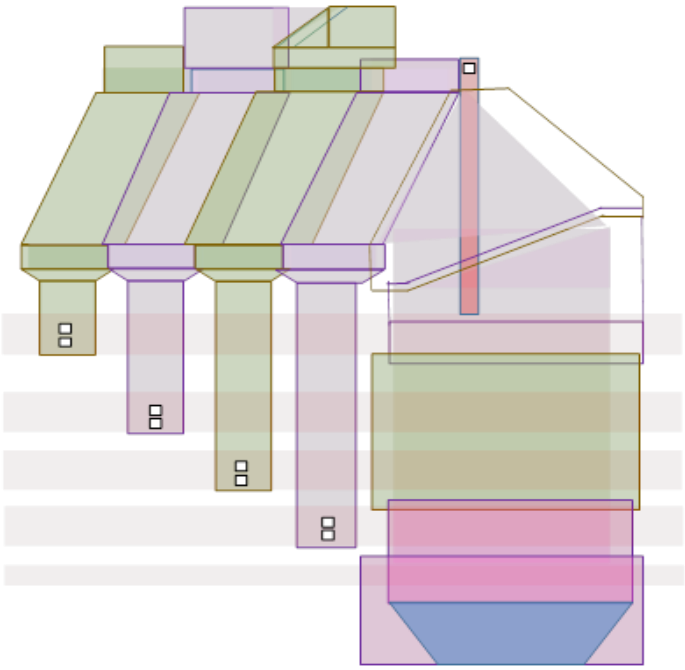


Figure 6. TAP / TILT HCCD Structure

Here the Tap/TILT structure or Horizontal shift Registers is bended so as to transfer the charge properly as the amplifiers cannot be directly connected to HSR and so it is designed accordingly due to so many amplifiers.

Hence the HSR is bended. The charge will be collected in 2nd and 3rd phase of HSR. Therefore, the bunch of two HSR is done so as to reduce the routing connection.

B. Output Section:

The output section comprises a floating diffusion charge detection node, a reset transistor and a two-stage N-buried channel source follower amplifier[3]. Floating diffusion is designed to give conversion gain of 5.35uV/e-.

Here the Floating diffusion capacitance can be calculated by summing the edge capacitance of OTG, reset gate, Tab capacitance, sidewall capacitance and depletion capacitance.

C. Routing:

There are 24 amplifiers in each array so the routing increases. The routing is very complex over here. There are approximately 470 pads.

The whole design in a chip will be covered by p+ guard ring so that external noise doesn't interrupt the design otherwise the pixels will get distorted.

The major care is taken while routing. Due to many amplifiers the array to array spacing increases. The pad connection is on all the sides of chip.

3. FUTURE SCOPE

As there are many amplifiers per array so as the routing becomes much complex; so it is been decided to reduce the no of pins because of that the array to array spacing, routing will get reduced but only the Amplifier readout rate will get increased.

This way the imaging sensor or TDI CCD is designed by taking care of all the appropriate considerations of designs and its capacitance and time constant. Hence, this device will be sent to fabrication process and then it will be tested as it works according to given requirements after the design.

4. CONCLUSION

Here, the TDI CCD imaging sensor which is designed of 13µm pitch by keeping the full well capacity of pixel and horizontal shift register accordingly.

Due to 24 amplifiers per array the device design becomes very complex and its dimension also increases as the readout rate of amplifier is 4.2MHz and so the array to array spacing also increases due to which routing increases and thus all this features has been achieved and designed properly.

Hence the TDI CCD will be majorly used for high resolution due to half pixel staggered and used to enhance the signal to noise ratio.

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