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Design and Simulation of GaAs MOSFET with High-K Dielectric Material

Vasudha Patil
M.Tech student. Department of Electronics and telecommunication, NMU, Jalgaon
Email: vasudhapatil28@gmail.com

Abstract: Analysis and characterization of the GaAs MOSFET with High-k gate dielectric material and also do the small signal analysis and noise analysis using TCAD tool. In present research work GaAs is employed as substrate material. Band gap of GaAs is about 1.43eV. Lattice constant for GaAS is 5.65A. Substrate doping is 1x10^16 cm-3. HFO2 gate dielectric deposited on GaAs (100) substrate. HFO2 film is 20nm thick. Dielectric constant of HFO2 is order of 20-25. Permittivity (F cm^-2) is 20€0. Band gap (eV) is 4.5-6.0.HFO2 grown by Atomic Layer Deposition on GaAs. The transition metal Au is proposed dopant for GaAs. Source/Drain junction depth is 20nm. Doping levels of drain source are 1e20. Gold is used for gate metal. A working GaAs device is simulated and out performs the Si core device due to its increased mobility. It also decreases leakage current. Solve the problem of Fermi level pinning. So GaAs MOSFET is always better than Si MOSFET.

Keywords: GaAs MOSFET,TCAD,HFO2Gate.

1. INTRODUCTION

1.1Basic MOS capacitance structure

Metal-Oxide-Semiconductor (MOS) capacitors are the heart of every digital circuit such as single memory chip, dynamic random-access memory (DRAM), switched capacitor circuits, analog-to-digital converters and filters, optical sensors and solar cells. A schematic view of a MOS capacitor is shown in the Fig.1.The MOS capacitor is parallel plate capacitor with silicon (S) as one electrode and the metal (M) as the other electrode. The insulator is generally an oxide (O) layer of silicon. The metal electrode is also known as the gate of the system. The silicon has an ohmic contact to provide an external electric contact. The thickness of the insulator (oxide) layer is denoted by d, and it determines the capacitance of the MOS capacitor. VG is the voltage applied to the gate of the MOS capacitors.

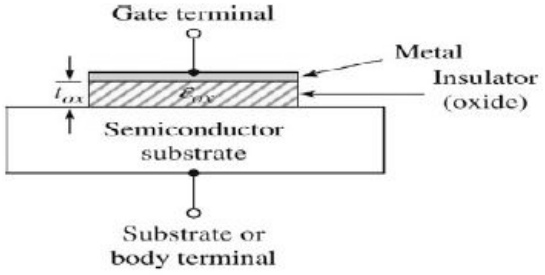

Fig.1: Basic MOS capacitance structure

Compound III-V materials are attractive for achieving enhanced n-FET mobility, due to their high bulk electron mobility. III-V channel n-MOSFETs can achieve performance enhancement as well as reduced dynamic power consumption for a fixed performance level. Si CMOS technology has been driven by device scaling to increase performance, as well as reduce cost and maintain low power consumption. However, as devices are scaled below the 100nm region, performance gain has become increasingly difficult to obtain by traditional scaling. High mobility materials can greatly improve the power performance tradeoff which is a tremendous advantage for VLSI digital applications. Currently in industry, mobility enhancement is achieved by applying strain to conventional Si MOSFETs, either through process-induced strain or substrate engineering. However, the mobility benefits that can be achieved by staining Si are limited and reduced by scaling, and there is great interest in studying non-Si channel materials to achieve even higher motilities. For gate materials, traditional SiO2 is being replaced by High-k dielectric to reduce the gate leakage current.

1.2 GaAs used as substrate

GaAs is the most common in use after silicon. III-V compound semiconductor is use due to their outstanding electron transport properties, their relative maturity and demonstrated reliability when compared with other candidates, such as carbon nanotube transistors and semiconductor nanowires. Moreover, it is well known that III-V-based MOSFETs usually have relatively low thermal tolerance in the device fabrication process. For instance, the interface between the gate oxide and III-V materials can be easily

degraded during high temperature processes such as the annealing step after ion-implantation in conventional inversion-mode MOSFETs. The amount of energy required for an electron to move from the valence band to the conduction band depends on temperature, the semiconductor material and material's purity and doping profile. For undoped GaAs, the energy band gap at room temperature is 1.42eV. The electron affinity for GaAs is 4.07 eV. GaAs have several advantages over Si for operation in the microwave region-primary, higher mobility and saturated drift velocity and the capacity to produce devices on a semi-insulating substrate.

2. INTRODUCTION TO SILVACO TCAD TOOL

2.1 Process Simulator-ATHENA

ATHENA: A Two-Dimensional Process Simulation Framework is a comprehensive software tool for modeling semiconductor fabrication process. ATHENA provides facilities to perform efficient simulation analysis that substitute for costly real world experimentation. ATHENA combines high temperature process modeling such as impurity diffusion and oxidation, topography simulation, and lithography simulation in a single, easy to use framework.

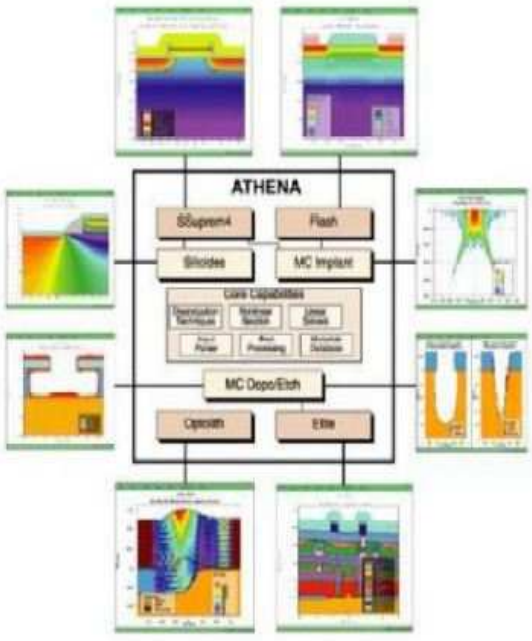

Fig.2: Athena Framework

2.3 Device Simulator-ATLAS

ATLAS is a physically based two and three-dimensional device simulator. It predicts the electrical behavior of specified semiconductor structure, and provides insight into the internal physical mechanisms associated with device operation. ATHENA is frequently used in conjunction with the ATLAS device simulator. ATHENA predicts the physical structure that result from processing .these physical structure are used as input b ATLAS, which then predicts the electrical characteristics associated with specified bias condition. The combination of ATHENA and ATLAS makes it straightforward to determine the impact of process parameter on device characteristics.

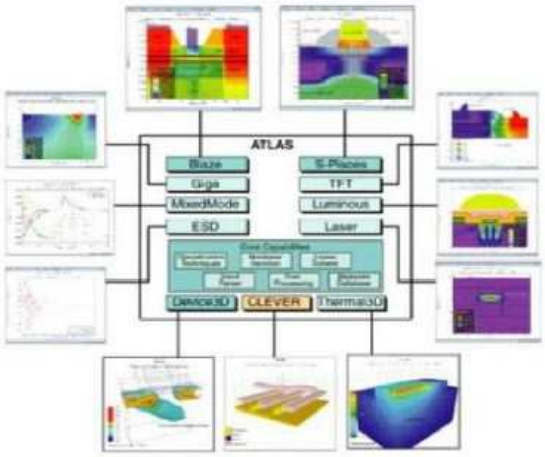

Fig.3: Atlas Framework

2.3.1 Inputs and Outputs of Atlas

Figure shows the types of information that flow in and out of ATLAS. Most ATLAS simulation use two input: a text file that contains commands for ATLAS to execute, and a structure file that defines the structure that will be simulated. ATLAS produces three types of output. The run time output provides a guide to the Progress of simulation running, and is where error messages and warning message appear. Log files. store summaries of electrical output information, and solution files store two and three dimensional data relating to the values of solution variables within the device.

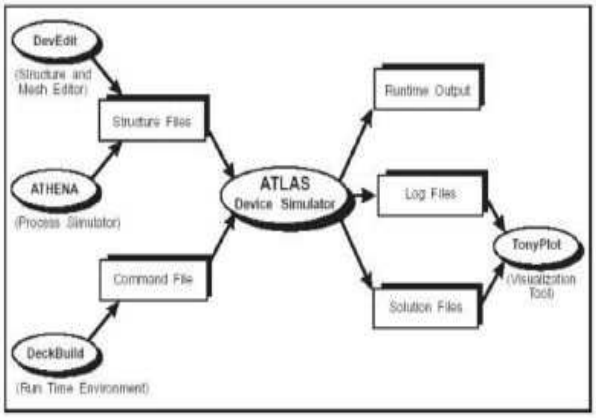

Fig: 4. Types of information that flow in and out of ATLAS

Yanning sun, S.J.Koester, E.W.Kiewra,[1] they worked on the benefits, the opportunities and challenges of III-V group compound semiconductor

for digital application. Also demonstrated functional enhancement mode of III-V group compound semiconductor. They concluded that The III-V group compound semiconductors have received renewed attention as the channel materials due to their high bulk electron mobility. K.Taff,T.R.Harris, el.[2]they worked on the electrical properties of GaAs are contracted to a Si device adhering to the ITRS 2008 road map using the Isetcad software package. They concluded that By combining short channel MOSFET with high-k dielectric allow the realization of high drive current minus the gate leakage current present in a classical Sio2 dielectric layer. Due to higher mobility bulk material whose characteristics, such as band gap & mobility have a direct influence on Ion & Ioff. C.H.Hsu, P.Chang, W.C.Lee,Z.K.Yang, Y.J.Lee.,[3] they worked on The HFO2/GaAs hetero structures with the oxide stacks prepared by two step MBE growth has an automatically sharp interface and no interfacial oxide layer. They conclude that the film, even with a gate thickness as thin as 1.8nm are made of monoclinic HFO2 of highly epitaxial quality. G.Lu.A.Facchetti,T.J.Marks,[4] they worked on Direct current and radiofrequency Characteristics of GaAs MISFET with very thin self-assembled organic nanodielectrics (SANDS) are presented. The application of SAND on compound semiconductor offer unique opportunity for high performance device. They concluded that Suggest the good opportunities for manipulating the complex GaAs surface chemistry with unprecedented material options and for using organic dielectrics for high performance III-V group semiconductor device.Prof.C.Hunt. [5] they worked on Oxide surface passivation grown by ALD has been applied to GaAs MESFETs using Al2O3 and HFO2 gate dielectric. They concluded that Both ALD grown Al2O3 and HFO2 passivation on the S-G and D-G spacing of MESFETs can significantly improve the breakdown characteristics of the devices. Al2O3 /HFO2 passivation without precleaning yields the best performance & Al2O3 /HFO2/GaAs interface is of high quality as passivation. It is applicable for power devices.

3. Problem formulation

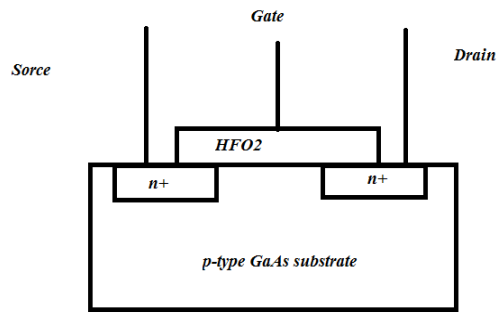

Fig.5: Basic structure of n-MOSFET

Analysis and characterization of the GaAs MOSFET with High-k gate dielectric material and also do the small signal analysis and noise analysis using TCAD tool. Here, GaAs is used as substrate material. Band gap of GaAs is about 1.43eV. Lattice constant for GaAS is 5.65A. Substrate doping is 1x10^16 cm-3. HFO2 gate dielectric deposited on GaAs (100) substrate. HFO2 film has 20nm thick. Dielectric constant of HFO2 is order of 20-25. Permittivity (F cm^-2) is 20€0. Band gap (eV) is 4.5-6.0.HFO2 grown by Atomic Layer Deposition on GaAs. The transition metal Au is proposed dopant for GaAs. Source/Drain junction depth is 20nm. Doping levels of drain source are 1e20. Gold is used for gate metal.

4. CONTRIBUTORY WORK (PART-I)

In this section, there is formation of MOS Capacitor structure in TCAD tool having following specifications:
GaAs–Doping concentration= 1x10^16cm^-3
HFO2- 20nm by atomic layer deposition
Titanium- Gate metal
Frequency-100MHz

4.1 MOS Capacitor

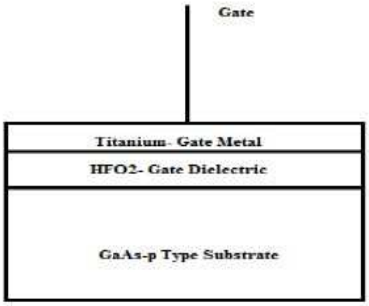

Fig: 6. MOS Capacitor

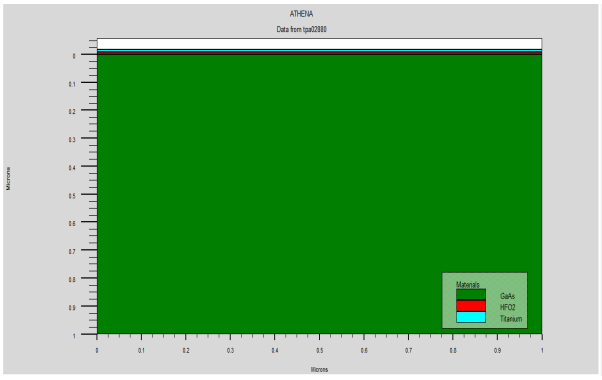

Fig: 7. MOS Capacitor structure in TCAD

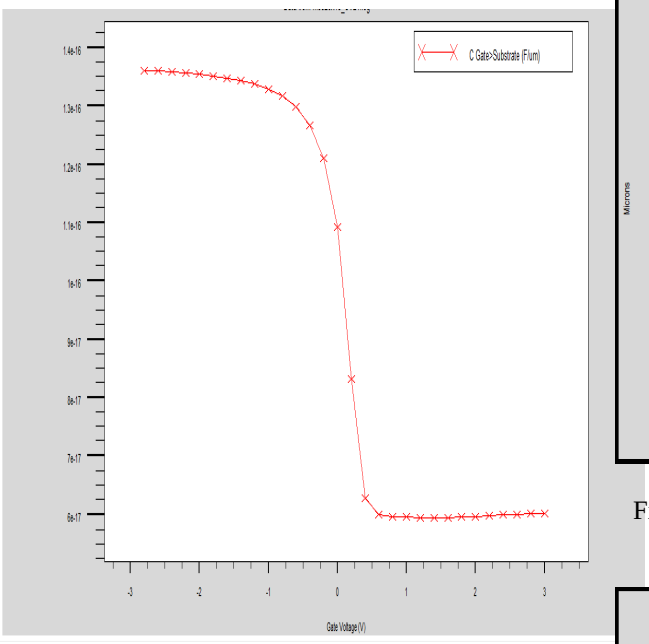

Fig: 8. C-V Characteristics of MOS Capacitor structure

Fig.7 shows MOS Capacitor structure in TCAD tool. This MOS capacitor having GaAs substrate with doping concentration= $1x10^{16}cm^{-3}$. HFO_2 is used as dielectric material. 20nm HFO_2 is deposited on GaAs by atomic layer deposition. Titanium is Gate metal.

Fig. 8 shows the C-V Characteristics of MOS Capacitor structure at 100MHz frequency. This characteristics measure at high frequency. It shows three regions accumulation, depletion, inversion. Fig8. Indicates the capacitance in accumulation region is $1.4X10^{-16}F$ at gate voltage -3V to 0V, in depletion region it decreases from $1.2X10^{-16}F$ to $6X10^{-17}F$ at range 0 to 0.3V gate voltage & in inversion region capacitance is $6X10^{-17}F$ at the range 0.3 to 3 V gate voltage .

5. CONTRIBUTORY WORK (PART-II)

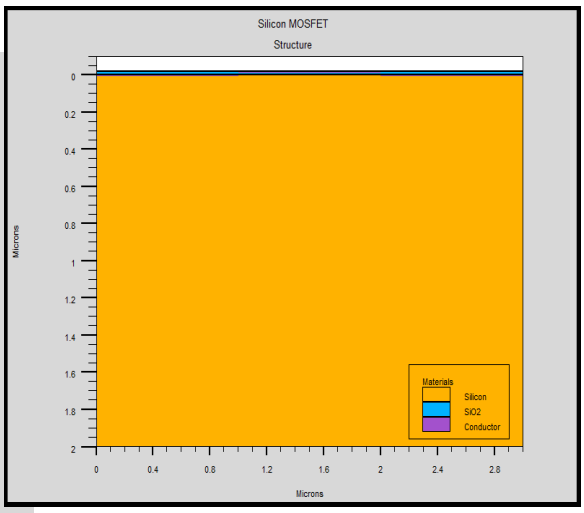

Fig: 9. Si MOSFET structure in TCAD of Lg=1µm.

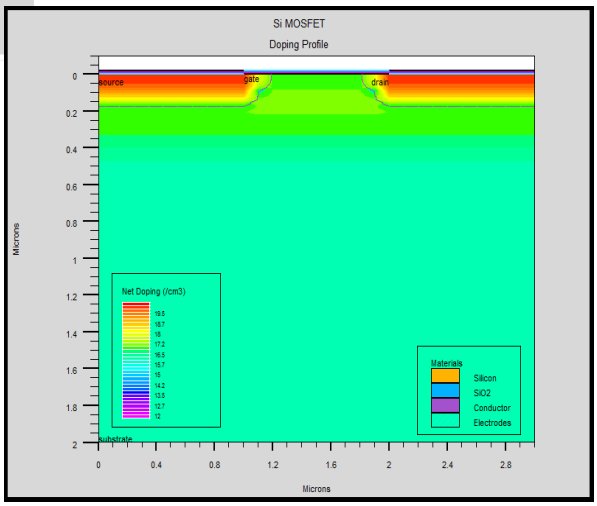

Fig: 10. Net doping of MOSFET

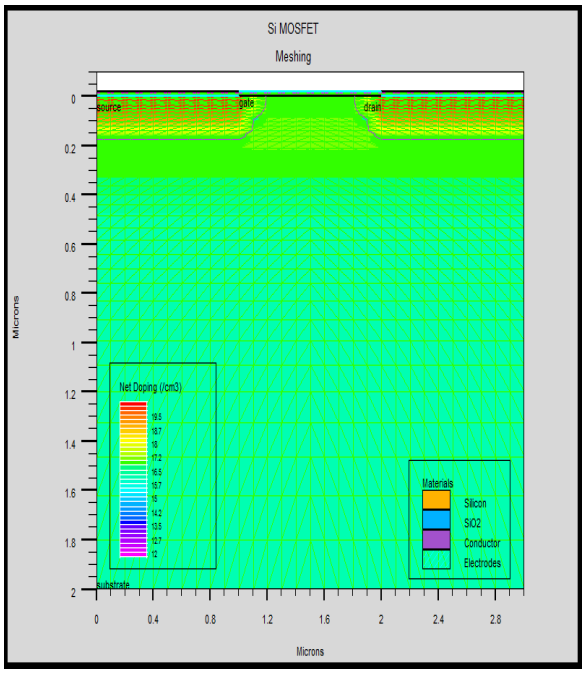

Fig: 11. Mashing of Si MOSFET

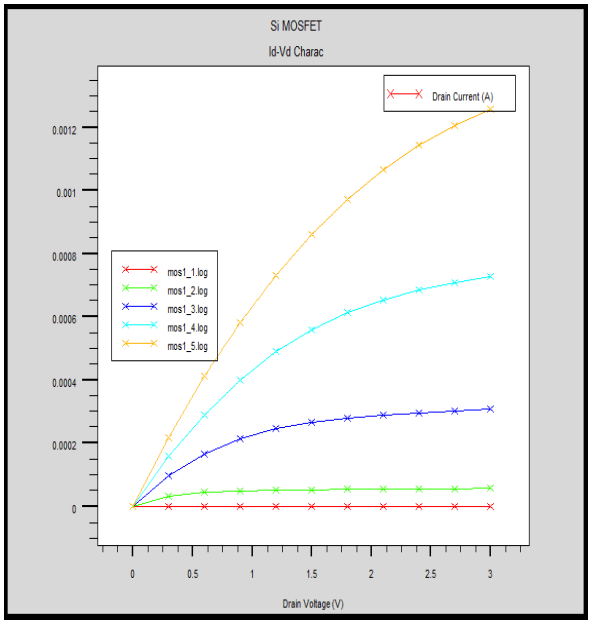

Fig: 12. Id-Vd Characteristics of Si MOSFET

5.1 Id-Vd Characteristics for Lg=1µm of Si MOSFET

Simulated DC Output Characteristics of Si MOSFET is Shown in fig 12. Drain current (Id) versus drain bias voltage (Vds) as a function of gate bias (Vgs) for SiO_2 (20nm) /Si MOSFET with 1µm gate length. The maximum drain current is 0.0 mA at 1V drain bias and 1V gate bias. Current is 0.066 mA at 1V drain bias and 2.0 gate bias. Current is 0.21 mA at 1V drain bias and 3.0 gate bias. Current is 0.73 mA at 1V drain bias and 4.0 gate bias. Current is 1.2 mA at 1V drain bias and 5.0 gate bias.

5.2 Id-Vg for Si MOSFET

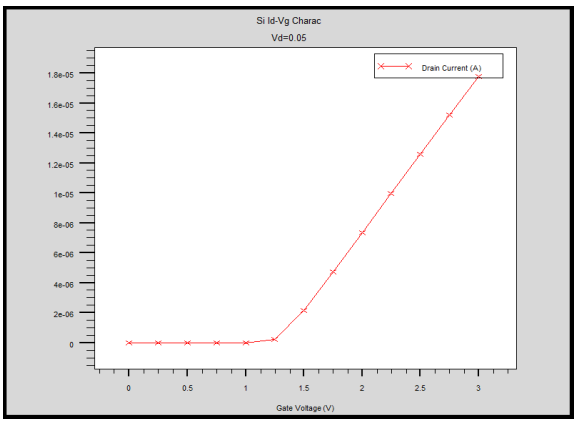

Fig: 13. Id-Vg for Si MOSFET Vd = 0.05V

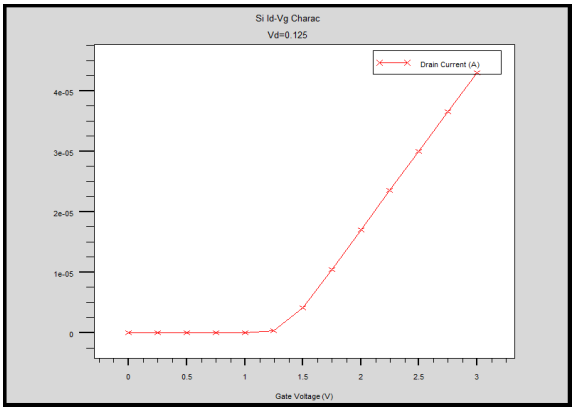

Fig: 14. Id-Vg for Si MOSFET Vd = 0.125V

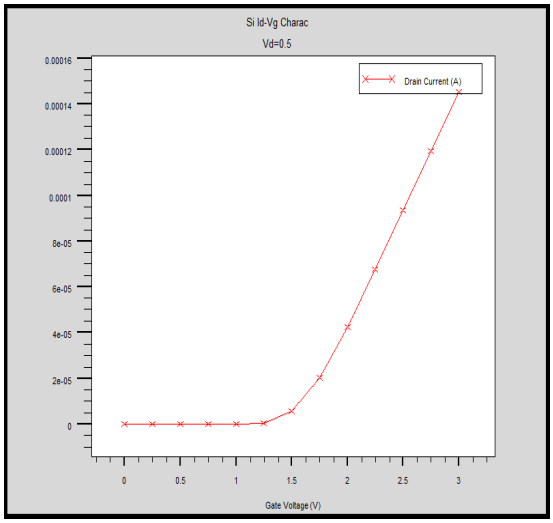

Fig: 15. Id-Vg Characteristics of Si MOSFET Vd=0.5V

5.3 Id-Vg Characteristics for Lg=1µm

Simulated DC Output Characteristics of Si MOSFET is Shown in above figures Drain current (Id) versus gate bias voltage (Vgs) as a function of drain bias(Vds) for SiO_2 (20nm) /Si MOSFET with 1µm gate length.The maximum drain current is 0.18µA at 0.05V drain bias and 1.0 gate bias in fig.13, the maximum drain current is 0.45 µA at 0.125V drain bias and 1.0 gate bias in fig.14. The maximum drain current is 0.14mA at 0.5V drain bias and 1.0 gate bias in fig.15.

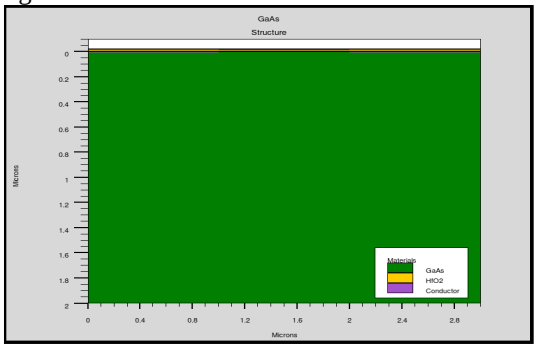

Fig: 16. GaAs MOSFET Structure in TCAD

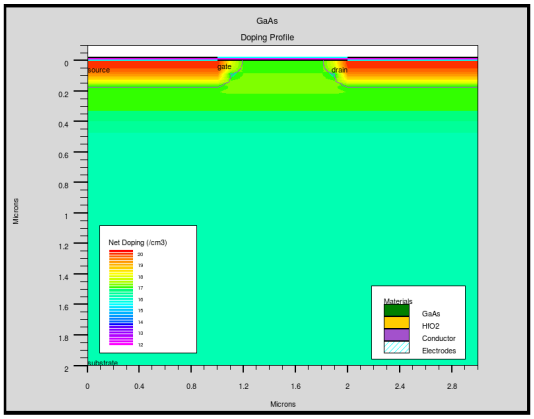

Fig: 17. GaAs MOSFET Structure with Net doping

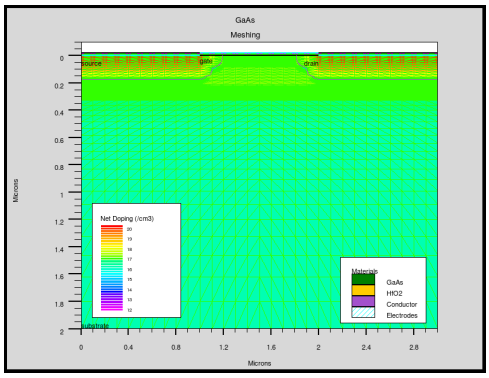

Fig: 18. GaAs MOSFET Meshing Structure

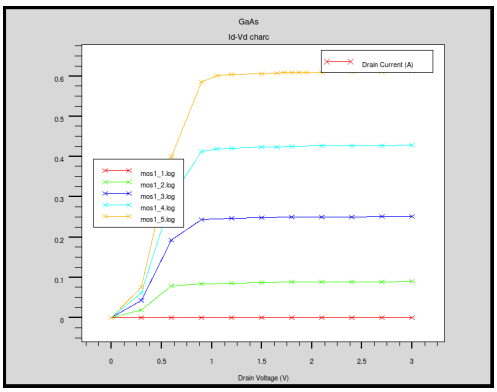

Fig: 19. Id-Vd Characteristics of GaAs MOSFET

5.4 Id-Vd Characteristics for Lg=1µm of GaAs MOSFET

Simulated DC Output Characteristics of GaAs MOSFET is Shown in fig 19. Drain current (Id) versus drain bias voltage (Vds) as a function of gate bias (Vgs) for HfO_2 (20nm) /GaAs MOSFET with 1µm gate length.The maximum drain current is 0 at 1V drain bias and 1V gate bias.Current is 0.075A at 1V drain bias and 2.0 gate bias.Current is 0.025 A at 1V drain bias and 3.0 gate bias.Current is 0.4 A at 1V drain bias and 4.0 gate bias.Current is 0.6 A at 1V drain bias and 5.0 gate bias.

5.5 Id-Vg Characteristics of GaAs MOSFET

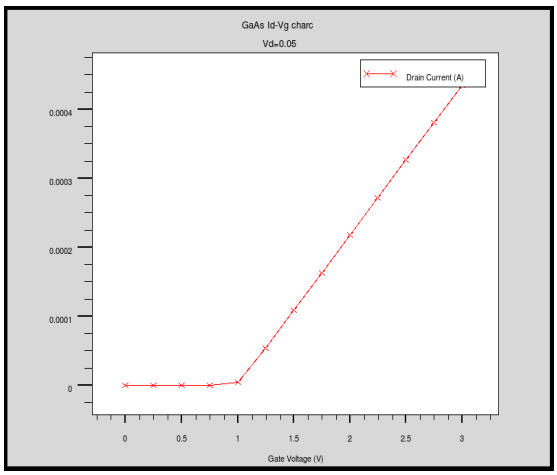

Fig: 20. Id-Vg Characteristics GaAs MOSFET for Vd=0.05V

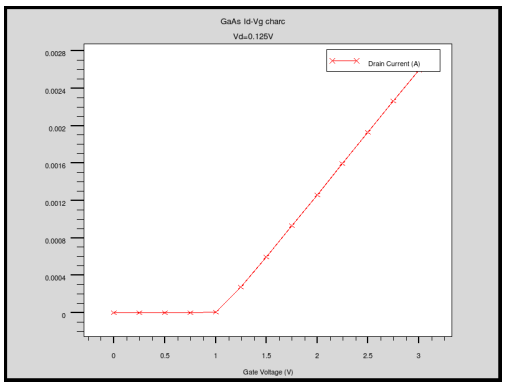

Fig: 21.Id-Vg Characteristics of GaAs MOSFET Vd=0.125V

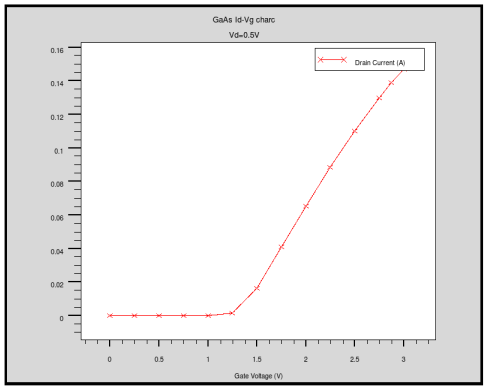

Fig: 22. Id-Vg Characteristics of GaAs MOSFET Vd=0.5V

5.6 Id-Vg Characteristics for Lg=1µm

Simulated DC Output Characteristics of GaAs MOSFET is Shown in above figures. Drain current

(Id) versus gate bias voltage (Vgs) as a function of drain bias (Vds) for HfO_2 (20nm) /GaAs MOSFET with 1µm gate length.The maximum drain current is 0.4mA at 0.05V drain bias and 1.0 gate bias in fig.20, the maximum drain current is 2.8mA at 0.125V drain bias and 1.0 gate bias in fig.21, the maximum drain current is 0.15A at 0.5V drain bias and 1.0 gate bias in fig.22.

5.6.1 Y- Parameter of GaAs MOSFET

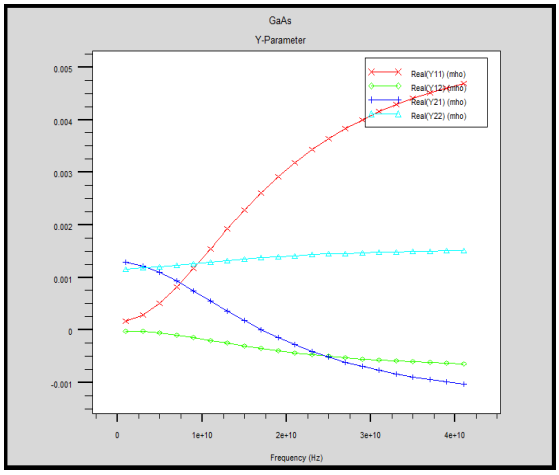

Fig. 23 Y- Parameter of GaAs MOSFET in TCAD

Y11= I/p conductance = (4.69e-003, 5.12e-003)
Y12= I/p conductance = (-6.51e-004, -1.77e-003)
Y21= Trans conductance = (-1.03e-003, -2.54e-003)
Y22= conductance = (1.51e-003, 2.34e-003)

5.6.2 S-Parameter of GaAs MOSFET

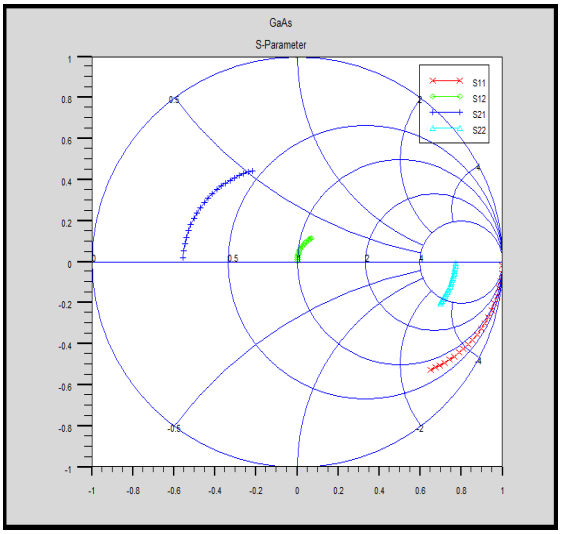

Fig.24 S-Parameter of GaAs MOSFET in TCAD

S11=(6.51e-001, -5.27e-001)
S12=(6.80e-002, 1.14e-001)
S21=(-2.18e-001, 4.44e-001)
S22=(6.96e-001, -2.03e-001)

6. Results and discussion

Sr.No.	Gate Vtg. (Vds=1V)	Si MOSFET(Id)	GaAs MOSFET(Id)
1	1V	0	0
2	2V	0.066mA	0.075A
3	3V	0.21mA	0.025A
4	4V	0.73mA	0.4A
5	5V	1.2mA	0.6A

Table: 4.Comparison table of Id-Vd Characteristics of Si and GaAs MOSFET

Above table. 4 shows comparison of Id-Vd Characteristics of Si and GaAs MOSFET. In this, the maximum drain current of Si MOSFET is 0.0 mA at 1V drain bias and 1V gate bias & for GaAs MOSFET drain current is 0.0 mA at 1V drain bias and 1V gate bias. The maximum drain current of Si MOSFET is 0.066 mA at 1V drain bias and 2V gate bias & for GaAs MOSFET drain current is 0.075A at 1V drain bias and 2V gate bias. The maximum drain current of Si MOSFET is 0.21mA at 1V drain bias and 3V gate bias & for GaAs MOSFET drain current is 0.025A at 1V drain bias and 3V gate bias. The maximum drain current of Si MOSFET is 0.73mA at 1V drain bias and 4V gate bias & for GaAs MOSFET drain current is 0.4A at 1V drain bias and 4V gate bias. The maximum drain current of Si MOSFET is 1.2 mA at 1V drain bias and 5V gate bias & for GaAs MOSFET drain current is 0.6 A at 1V drain bias and 5V gate bias. From above table, it is observe that in each case drain current of GaAs MOSFET is always greater than that of Si MOSFET.

Sr. No.	Drain Vtg. (Vgs=1V)	Si MOSFET(Id)	GaAs MOSFET(Id)
1	0.05V	0.18µA	0.4mA
2	0.125V	0.45µA	2.8mA
3	0.5V	0.14mA	0.15A

Table: 5. Comparison table of Id-Vg Characteristics of Si and GaAs MOSFET

Above table.5 shows comparison of Id-Vd Characteristics of Si and GaAs MOSFET. In this,the maximum drain current of Si MOSFET is 0.18µA at 0.05V drain bias and 1.0 gate bias in fig.13 & the maximum drain current for GaAs MOSFET is 0.4mA at 0.05V drain bias and 1.0 gate bias in fig.20. The maximum drain current of Si MOSFET 0.45 µA at 0.125V drain bias and 1.0 gate bias in fig.14 & the maximum drain current for GaAs MOSFET is 2.8mA at 0.125V drain bias and 1.0 gate bias in fig.21. The maximum drain current of Si MOSFET 0.14mA at 0.5V drain bias and 1.0 gate bias in fig.15 & the

maximum drain current for GaAs MOSFET is 0.15A at 0.5V drain bias and 1.0 gate bias in fig.22.

7. CONCLUSION

GaAs is the most common in use after silicon. III-V compound semiconductor is use due to their outstanding electron transport properties, their relative maturity and demonstrated reliability when compared with other candidates, such as carbon nanotube transistors and semiconductor nanowires. Moreover, it is well known that III-V-based MOSFETs usually have relatively low thermal tolerance in the device fabrication process. For instance, the interface between the gate oxide and III-V materials can be easily degraded during high-temperature processes such as the annealing step after ion-implantation in conventional inversion-mode MOSFETs.

A working GaAs device is simulated and outperforms the Si core device due to its increased mobility. It also decreases leakage current. Solve the problem of Fermi level pinning. So GaAs MOSFET is always better than Si MOSFET.

Acknowledgement

Author wish to express deep appreciation to Mr. D. K. Gautam Sir and Mrs. Prerana Jain Madam, for their motivation and guidance. Their guidance has been invaluable to the completion of this project work.

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