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Comparison of 24X24 Bit Multipliers for Various Performance Parameters

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Abstract: This paper contains comparison of the four 24X24 bit unsigned multipliers are done for the various performance parameters. The multipliers included in this comparison are array multiplier, radix 4 booth multiplier, wallace tree multiplier and vedic multiplier. All multiplier designs were modeled in Verilog HDL and synthesized based on the TSMC 180nm standard cell library. Comparisons are based on the synthesis result obtained by synthesizing all the multiplier using Cadence RTL Compiler Ultra.

Keywords – Array Multiplier , Wallace Tree Multiplier , Vedic Multiplier , Modified Booth Multiplier

1. INTRODUCTION

Multipliers are an crucial part of the modern electronic era. Multipliers can found electronics systems that run complex calculations especially in DSP processor, Microcontroller and Microprocessor. Many transform algorithms like Fast Fourier transforms (FFTs), DFT etc make use of multipliers [5], [6], [7].Due to this reason several analyses have been on different multiplier architectures which aided the designers to further develop the multiplier technology . In parallel multipliers the number partial product addition required determines the performance for the multipliers.

Previous performance parameter comparison have been conducted on multiplier designs such as Array Multiplier , Wallace tree multiplier and Booth Multiplier. A study in [1] using TSMC 0.35 micron standard library showed that array multiplier has the largest area and delay when compared to other multiplier design , while the Wallace tree multiplier has less area and delay compared to the array multiplier . In [2] the study was targeted towards Xilinx FPGA 4052XL-1HQ240C , stated that depending on the application either booth multiplier and wallace multiplier since Booth Multiplier uses less area compared to wallace tree multiplier but wallace tree multipliers dissipates less power . In study [3] targeting Xilinx device family Spartan3, package tq144 and speed grade -5 , stated that in Vedic Multiplier when ripple carry adder is used the area required is less compared to the use of carry save adder . Booth Multiplier is the best when compared to other multiplier [4].

2. ARRAY MULTIPLIER

Array Multiplier is one of the best known and simplest multipliers. The multiplier is based on the shift and add algorithm. The partial products are generated by multiplying the multiplicand with one bit of the multiplier. The partial product is then shifted to the left in the order of the multiplier bit and then the partial products are added to give the final result.

Figure 1. shows the basic principle of the 4X4 array multiplier. Here the LSB of the first partial product becomes the LSB of the product and the rest of the bits of the partial product is added to the second shifted partial product. The LSB of the addition becomes the next Bit of the product. This process is followed till the last partial product is added to the sum of the previous addition and the result of this addition is then placed in the product .

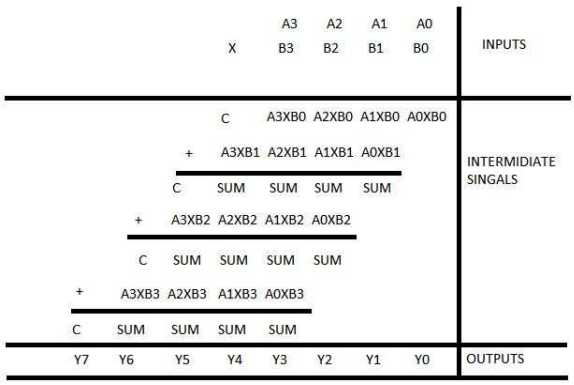

Fig. 1: Operation Of 4X4 Array Multiplier

3. WALLACE TREE MULTIPLIER

Wallace introduced an efficient multiplication algorithm[8] , which has a reduced delay in order of

O(log n) . The logarithmic increase in delay with respect to operand size provides speed gain over array multiplier which has a linear increase in delay .
In this multiplier architecture all the bits of all the partial products in a column are added together in parallel without the propagation of any carries . The process is repeated till there is only two rows of the matrix is left , the two rows are then added using a fast adder . Here a 3:2 compressor is used which is based on carry save adder .
The matrix for each stage with its height for a 8X8 wallace tree multiplier is shown Figure 2.

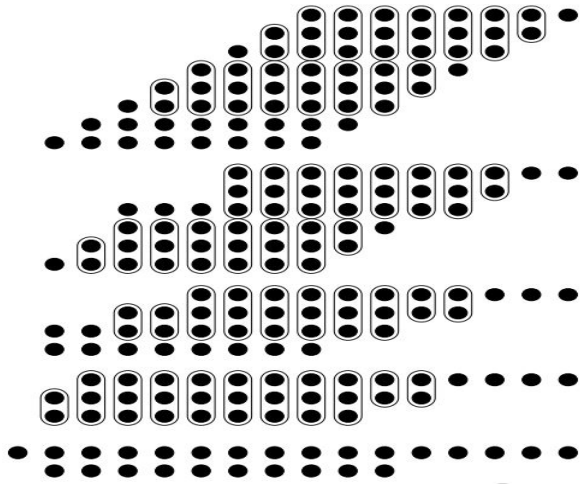

Fig. 2: Reduction in 8X8 Wallace Tree Multiplier

4. MODIFIED (RADIX 4) BOOTH MULTIPLIER

The radix 4 booth multiplier also known as modified booth algorithm [9] is a well know technique which is used to reduce the partial product generated for the addition when two numbers are multiplied . In radix 4 technique , 3 bit encoding is used due to which the number of partial products are half.

3 Bit Encoding	Operation to be performed
000	Zero is multiplied to multiplicand
001	+1 is multiplied to the multiplicand
010	+1 is multiplied to the multiplicand
011	+2 is multiplied to the multiplicand
100	-2 is multiplied to the multiplicand
101	-1 is multiplied to the multiplicand
110	-1 is multiplied to the multiplicand
111	Zero is multiplied to the multiplicand

Table 1: Radix 4 Booth Encoding Scheme

Depending on the 3 bit encoding some operation are performed on the multiplier before it becomes the partial product . These operation are given in Table 1 . After the operation are performed on the multiplicand ,the resulted is twice to left depending on the order of the encoded bits. Finally the partial products are added together to give product.

5. VEDIC MULTIPLIER

Vedic multiplier is based on the vedic multiplication sutra. These sutras are used for the multiplication of two numbers in decimal system . We have applied the same principal on the binary number system and design the multiplier .
The multiplier is based on Urdhava Triyakbhayam Sutra [10] . In this concept the generation of partial product can be done and then parallel addition of these partial product is done .

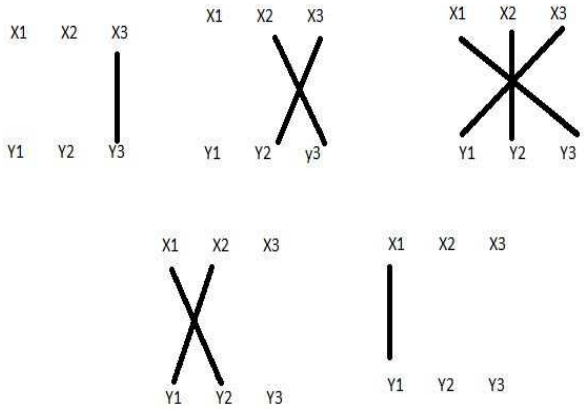

Fig. 3: Vedic Multiplication Technique

For an example let us take a 3X3 multiplier which is shown in Fig. 3. Consider the numbers X and Y where A = X1X2X3 and Y= Y1Y2Y3. The LSB of X is multiplied with the LSB of Y:
Su0=X3Y3;
Then X3 is multiplied with Y2, and Y3 is multiplied with X3 and the result are added together as:
Ca1Su1 = X3Y2 + X2Y3
Here Ca1 is carry and Su1 is sum. Next step is to add Ca1 with the multiplication results of X3 with Y1, X2 with Y2 and X1 with Y3:
Ca2Su2=Ca1+X1Y3+X2Y2 + X3Y1
Next step is to add Ca2 with the multiplication results of X1with Y2 and X2 with Y1 : Ca3Su3=Ca2+X1Y2+X2Y1
Similarly the last step is :

Ca4Su4=Ca3+X1Y1
Now the final result of multiplication of X and Y is Ca4Su4Su3Su2Su1Su0.
The 24X24 bit multiplier is design by using four 12X12 bit multiplier . The 12X12 Multiplier is again designed using four 6X6 multiplier . The 6X6 Multiplier is again designed using four 3X3 multiplier. So the multiplier uses hierarchical structure to reduce the number of partial product generation . Figure 4 shows the design of the 24X24 bit multiplier.

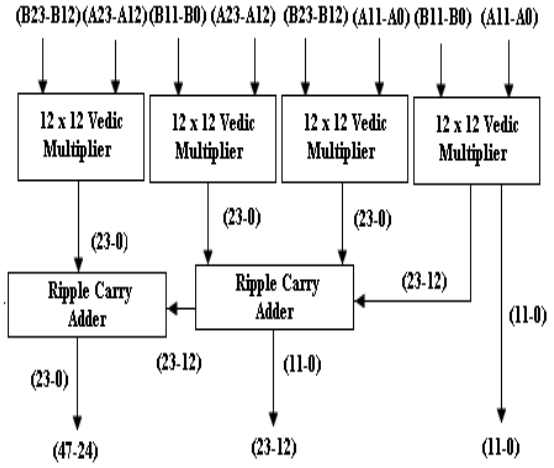

Fig. 4: 24X24 Bit Vedic Multiplier

6. RESULTS AND DISCUSSIONS

A. Area Comparison

Array multiplier uses the largest area, followed by Wallace tree multiplier with a reduction of 19% over array multiplier. Vedic multiplier has a further reduction of 21 % over wallace tree and finally the best area result is obtained by Modified Booth multiplier with a reduction of 16%.

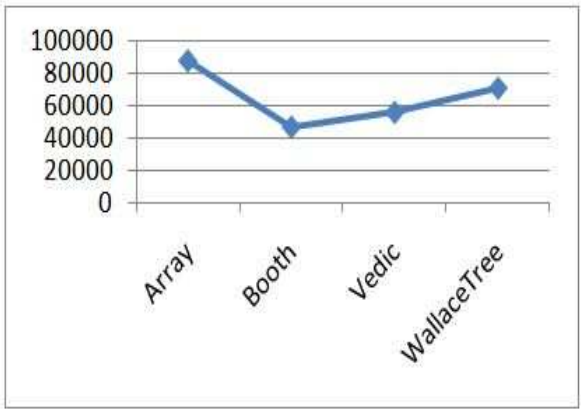

Fig. 5: Graph For Area Comparison

B. Delay Comparison

Booth multiplier gives the best result in respect with delay. Followed by vedic multiplier with an increase of 10.6% . Wallace tree multiplier is third best with an increase of 9.6 % over vedic multiplier . Finally the worst delay is shown in array multiplier with an increase of 39.26% over wallace tree multiplier .

C. Power Comparison

Vedic multiplier gives the best result in respect with power dissipation. Followed by booth multiplier with an increase of 20.26% . Wallace tree multiplier is third best with an increase of 21.38 % over booth multiplier . Finally the worst power dissipation is shown in array multiplier with an increase of 5.6%.

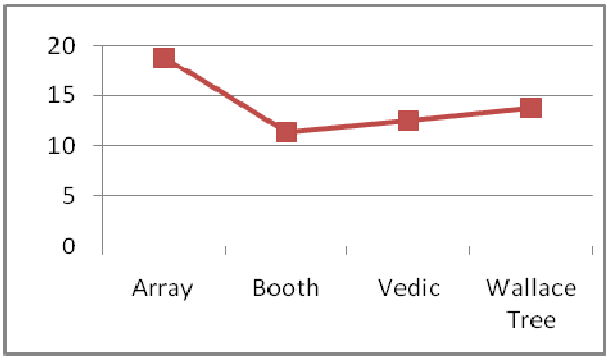

Fig. 6: Graph For Delay Comparison

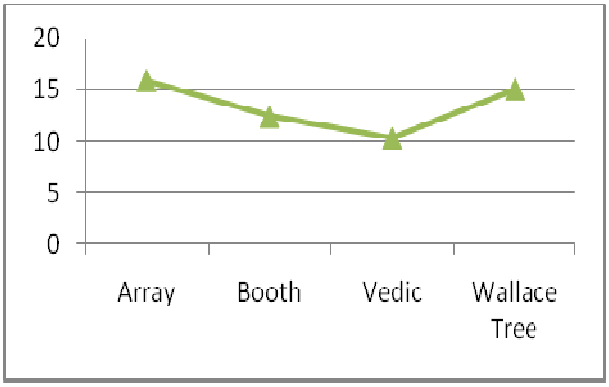

Fig. 7: Graph For Power Comparison

7. CONCLUSION

These four multiplier are based upon four distinct algorithm , each having its individual advantages and disadvantages .
Based on the experimental data gathered as seen in table 2, array multiplier although has a simple structure and mosteasy to implement but its performance is poor when compared to other multipliers. As discussed earlier it is seen that the

wallace tree multiplier has a better delay compared to array multiplier due to the use of carry save adder .
Depending on the application it can be stated that either modified booth multiplier or vedic multiplier can be used as a multilier . If the application requires a fast multiplier then booth multiplier (radix 4) can be used, on the other hand if low power multiplier is required then vedic multiplier can be used. Although booth multiplier has less area and delay but the vedic multiplier has a better power delay product and power density compared to booth multiplier .

Parameter	Array Multiplier	Booth Multiplier Radix 4	Vedic Multiplier	Wallace Tree Multiplier
Delay(ns)	18.8	11.3	12.5	13.7
Area	87707	46982	55999	70962
Power Dissipation (mw)	15.878	12.386	10.299	15.035
A.D(10^{-3})	1.649	0.531	0.700	0.972
P.D(10^{-15})	298.5064	139.9618	128.7375	205.9795
Power density(10^{-10})	1.810	2.636	1.840	2.119

Table 2 : Performance Parameter Of Four Multiplier

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